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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,957	07/16/2003	Robert Osann JR.	117928-156945	2024

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SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITE 1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
10/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/621,957	OSANN, ROBERT	
	Examiner	Art Unit	
	ANH Q. TRAN	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *4-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,9 and 11-18* is/are rejected.

7)☒ Claim(s) *3,10 and 19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Douglass (6,961,919).

Claim 1, Douglass shows a semiconductor device (Fig. 11) comprising a processor (fixed logic 1128 and 1129, processing circuit, col. 10, lines 29-31) having reprogrammable instructions implemented in field-programmable logic (programmable logic fabric 1110), wherein all I/O connections (I/Os 1161, 1171, 1191) for the field-programmable logic couple to the processor.

Claim 8, Douglass shows the semiconductor device of claim 1, wherein the processor comprises a DSP processor (digital signal processor, col. 5, lines 56-67).

3. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Douglass et al. (6,886,092).

Claim 2, Douglass shows a family of two or more ASIC devices (Figs. 4 and 5) comprising a processor having mask-programmable (mask, col. 3, lines 31-41)

instructions implemented in ASIC logic, wherein each device member of the family has different amounts of ASIC logic available (device of Fig. 5 had less amounts of ASIC logic available, e.g. programmable logic fabric 12 that is not configured yet, than figure 4 excluding programmed dedicated processors portions), and wherein each member of the device family has substantially identical processors (processors 62 and 16), processor memory (memory 18-24 and memory 64-70), and numbers of input/output connection (IOB 14).

4. Claims 9, 11-16, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato (6,826,674).

Claim 9, Sato shows an integrated circuit, comprising:

a fixed portion comprising one or more fixed logic blocks (43 which includes processor, registers, col. 11, lines 40-46);

a reprogrammable portion (DFU45) comprising a plurality of reprogrammable logic blocks (FPGAs); and

instruction logic (42) coupled to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks, wherein the instruction logic is configured to decode an instruction stream of a software program (39) to sequentially provide control signals to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks according to a sequence of execution of the software program (software, col. 15, line 33-35).

Claim 11, Sato shows the integrated circuit of claim 9, wherein the reprogrammable portion is subordinate to the fixed portion (DFU45 is subordinate).

Claim 12, Sato shows the integrated circuit of claim 9, wherein the fixed portion is a software-programmable digital signal processor (processor 43, col. 11, lines 40-46).

Claim 13, Sato shows the integrated circuit of claim 9, wherein the reprogrammable portion is a field-programmable gate array (FPGAs).

Claim 14, Sato shows the integrated circuit of claim 9, wherein substantially all of the plurality of reprogrammable logic blocks are identical (FPGAs are the same).

Claim 15, Sato shows the integrated circuit of claim 9, wherein the plurality of reprogrammable logic blocks (three paths and each path is consider a block, e.g. two paths each including 4 DPU and one path including 2 DPU of fig. 12b) include at least two different reprogrammable logic block types that differs by an amount of logic (two paths, each including 4 DPUs and one path including 2 DPU are different by amount of logic) and/or a type of logic.

Claim 16, Sato shows the integrated circuit of claim 9, wherein the reprogrammable portion further comprises at least one application-specific function block (CNT and RAMs).

Claim 18, Sato shows the integrated circuit of claim 9, wherein the fixed portion comprises the instruction logic (42 is fixed portion).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (6,826,674) in view of Langhammer (6,781,408).

Sato discloses the claimed invention except for the at least one application-specific function block is a Multiplier, Barrel Shifter, Bit-Reverse Address Generator, Auto-Scaling Unit, Large Multiplier, or Viterbi Decoder instead of the RAM. Langhammer discloses that it is known in the art to implemented the function specific blocks as: multiplier, barrel-shifter,... RAM, col. 1, lines 11-24).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the multiplier or the barrel-shifter with FPGA of Sato, in order to perform one or more specific tasks.

Allowable Subject Matter

7. Claims 3, 10, 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH Q. TRAN whose telephone number is (571)272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh Q. Tran/
Primary Examiner, Art Unit 2819
10/20/08